Enhancement-Mode Gate-Recess-Free GaN-Based *p*-Channel Heterojunction Field-Effect Transistor With Ultra-Low Subthreshold Swing

Chen Yang, Houqiang Fu, Prudhvi Peri, Kai Fu, Tsung-Han Yang, Jingan Zhou, Jossue Montes, David J. Smith, and Yuji Zhao, *Member, IEEE*

***Abstract*— We report enhancement-mode *p*-channel heterojunction field-effect transistors (HFETs) without gate recess on a standard *p*-GaN/AlGaN/GaN high electron mobility transistor (HEMT) platform. The *p*-GaN in the gate region was partially passivated by a low-power hydrogen plasma treatment process, and the remaining active *p*-GaN and the underlying AlGaN formed the *p*-channel. The device showed a record low off-state leakage of $<10^{-8}$ A/mm and subthreshold swing (*SS*) of 123.0 mV/dec with a threshold voltage (V_{th}) of −0.6 V and high-temperature stability up to 200 °C. These results indicate that the hydrogen plasma treatment is beneficial for suppressing leakages and preserving excellent material quality in the *p*-channel. With the success of the *p*-HFETs, the *p*-GaN/AlGaN/GaN platform can enable the monolithic integration of GaN *n*- and *p*-channel transistors without the need for regrowth. This work represents a significant step towards the implementation of the GaN CMOS technology.**

***Index Terms*— Gallium nitride, *p*-channel, heterojunction field-effect transistors, E-mode, leakage, subthreshold swing.**

I. Introduction

III-NITRIDE high electron mobility transistors (HEMTs) have shown superior performances in high-power and high-frequency applications due to their high critical electric field, polarization-induced high density of two-dimensional electron gas (2-DEG), high mobility, and high electron saturation velocity [1]–[3]. Recently, rapid progress has been made in developing GaN power integrated circuits (ICs) on cost-effective GaN-on-sapphire and GaN-on-silicon platforms [4], [5]. The success of III-nitride HEMTs has stimulated the research for their counterparts with the two-dimensional hole gas (2-DHG) channel [6]–[16]. The realization of complementary *n*-channel and *p*-channel III-nitride transistors can reduce the design complexity of power ICs, lower the static power consumption, and increase the logic swing.

As a critical component in GaN power IC technology, the *p*-channel devices are expected to deliver comparable ON-current density, low leakage, low subthreshold swing (*SS*), and compatible with existing *n*-channel devices. However, to date, there have been very few reports on the III-nitride *p*-channel devices, and their performance is still far from the material limit, especially for the off-state characteristics [17].

Several early reports demonstrated polarization-induced 2-DHG devices by engineering III-nitride heterojunctions, such as GaN/AlN [16], GaN/AlGaN [8], GaN/AlInGaN [10], and InGaN/GaN [6]. Recent works focused on the readily available commercial *p*-GaN gated HEMT platform, which is more suitable for CMOS integration. Regardless of the approach to generate the 2-DHG, the top layer in the devices is usually *p*-GaN to realize source and drain ohmic contacts, and a relatively thick *p*-GaN would be beneficial for lowering the contact resistance. On the other hand, the thick *p*-GaN layer in the gate region would lead to difficulties in pinching off the 2-DHG channel. A common solution to this issue is the recessed gate, where part of *p*-GaN under the gate is removed by dry etching. However, ion bombardment during dry etching could lead to damage in the gated region and *p*-channel, and create unwanted trap states, which may result in high off-state leakages, high *SS*, and reliability concerns [18]–[21]. Zheng *et al.* [12] demonstrated a post oxygen plasma passivation treatment, which suppressed the off-state leakages to $\sim 10^{-7}$ mA/mm and decreased the *SS* to 230 mV/dec. However, the off-state leakage and *SS* of *p*-channel devices are still high compared with *n*-channel devices, which presents a significant obstacle to GaN CMOS integration.

Hydrogen plasma treatment has been recently used in *p*-GaN gate HEMTs to realize the normally-off operation and suppress the off-state leakage [23]. The hydrogen plasma can passivate *p*-GaN, which can then be applied to various device

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Chen Yang, Kai Fu, Tsung-Han Yang, Jingan Zhou, Jossue Montes, and Yuji Zhao are with the School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ 85287 USA (e-mail: yuji.zhao@asu.edu).

Houqiang Fu is with the Department of Electrical and Computer Engineering, Iowa State University, Ames, IA 50011 USA (e-mail: houqiang@iastate.edu).

Prudhvi Peri is with the School for Engineering of Matter, Transport and Energy, Arizona State University, Tempe, AZ 85287 USA.

David J. Smith is with the Department of Physics, Arizona State University, Tempe, AZ 85287 USA.

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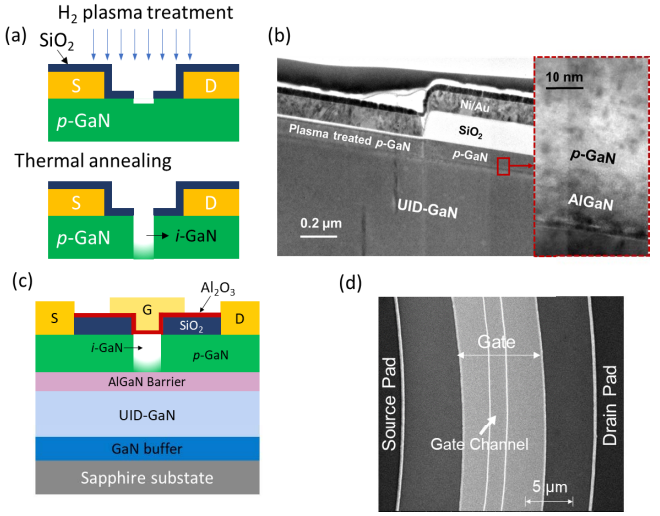

Fig. 1. (a) Schematic of the hydrogen plasma treatment process at the gated region. (b) TEM cross-section profile of the *p*-channel HFET (c) Schematic of the *p*-channel HFET. (d) SEM image of the gated region ($L_{GS}/L_G/L_{GD}$ = 8/2/8 μm).

designs [24]–[27]. In this work, we demonstrated *p*-channel heterojunction field-effect transistors (HFETs) using a *p*-GaN gate HEMT structure where the gate region was treated by hydrogen plasma instead of gate recess. The devices showed record low off-state leakage and *SS*. These results can serve as an important reference for *p*-channel GaN transistors and greatly benefit the development of III-nitride CMOS devices.

II. Device Fabrication

The *p*-GaN gated HEMTs were grown on a 6-inch GaN-on-sapphire wafer by metalorganic chemical vapor deposition (MOCVD). The structure consisted of a 90-nm *p*-GaN with an Mg concentration of 2×10^{19} cm^{-3}, a 15-nm $Al_{0.2}Ga_{0.8}N$ barrier, a 300-nm unintentionally doped GaN channel, and a GaN buffer layer. The 2-DHG formed at the *p*-GaN/$Al_{0.2}Ga_{0.8}N$ heterojunction interface served as the *p*-type channel. The hole sheet density was 1.48×10^{13}cm^{-2}, and the hole mobility was 11.9 cm^2/V·s as measured by Hall measurements.

The device fabrication started with the formation of *p*-GaN contacts at the source and drain. The source/drain regions were defined by photolithography and immersed in buffered oxide etchant (BOE) to remove native oxides. Metal stacks of Pd/Ni/Au (10 nm/20 nm/150 nm) were deposited by electron beam evaporation and annealed in nitrogen at 450 °C for 5 minutes. A layer of 150-nm-thick SiO_2 was then grown by plasma-enhanced chemical vapor deposition (PECVD), and a 2-μm gate window was opened by reactive ion etching (RIE). This layer served as both the passivation layer and the hard mask for hydrogen plasma treatment.

Figure 1(a) schematically illustrates the process of the two-step hydrogen plasma treatment. The sample was first exposed to the hydrogen plasma in the inductively coupled plasma (ICP) tool with an ICP at 300 W and an RF power at 5 W. The first step deposited hydrogen atoms near the surface. Then an additional 30-second rapid thermal annealing (RTA) at 400 °C was applied to drive the hydrogen atoms deeper and passivate the *p*-GaN. The diffusion process resulted in a gradient distribution of hydrogen atoms. With the

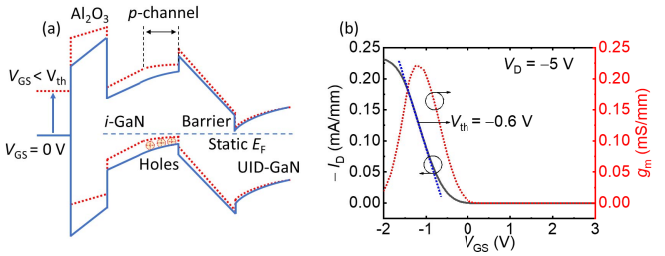

Fig. 2. (a) Energy band diagram under the gate region of the device at $V_{GS} = 0$ (OFF state) and $V_{GS} < V_{th}$ (ON state). (b) Linear scale transfer characteristics of the *p*-channel HFET showing the V_{th} of −0.6 V.

control of RTA temperature and time, the hydrogen plasma treatment was designed to only passivate the top portion of the *p*-GaN layer, while the underlying portion of *p*-GaN and the AlGaN barrier formed the conductive 2-DHG *p*-channel. Since the conventional gate recess process involves plasma dry etching, it can induce damage or trap states near the channel. The hydrogen plasma method used here provides a dry-etching-free process; thus, the *p*-channel will not be damaged and maintain high material quality.

The devices were then isolated by mesa etching, followed by a 10-nm Al_2O_3deposition by atomic layer deposition (ALD) as the gate dielectric. Gate metal stacks of Ni/Au (20 nm/100 nm) were then e-beam evaporated as gate electrodes. The devices were finished by the formation of the source and drain contact via opening. The effective sheet resistance and contact resistance were extracted to be 43.3 kΩ/□ and 76.0 Ω·mm, respectively, by the transmission line method (TLM). Figure 1(b) shows the cross-sectional profile of the as-fabricated *p*-channel HFET at the gate corner by TEM (transmission electron microscope). The schematic of the device is shown in Fig. 1(c) and the top-view scanning electron microscopy (SEM) image of the device gate region is shown in Fig. 1(d). The gate-to-source distance (L_{GS}), gate length (L_G), and gate-to-drain distance (L_{GD}) were 8 μm, 2 μm, and 8 μm, respectively.

III. Results and Discussion

Figure 2(a) illustrates the energy band diagram under the gate region of the device. It was reported that the hydrogen passivated *p*-GaN still maintains a single crystal structure with Fermi level located close to the middle of the bandgap [24]. At zero bias, due to the depletion effect, there are insufficient holes in the channel for conduction. At a negative bias, the Fermi level of the channel is moved upward with increased hole concentration. Therefore, this device operates as an enhancement-mode (E-mode) *p*-FET with a negative threshold voltage (V_{th}). The transistor characteristics were measured by a Keithley 4200 SCS semiconductor parameter analyzer. Figure 2(b) shows the transfer curve $I_D - V_{GS}$ and the transconductance curve $g_m - V_{GS}$ of the *p*-GaN HFET in a linear scale. The $V_{th}$was extracted by linear extrapolation at the maximum transconductance of $I_D - V_{GS}$ curve. This device exhibited a negative V_{th} of −0.6 V and a peak transconductance (g_m)of 0.22 mS/mm.

Figure 3(a) shows the transfer curve and the gate current of the devices in a semi-log scale. The transfer curve of the devices exhibited a high ON/OFF ratio of $\sim 5 \times 10^7$, and the drain leakage of the device was below 10^{-8} mA/mm (close to the setup limit), which is a record low leakage

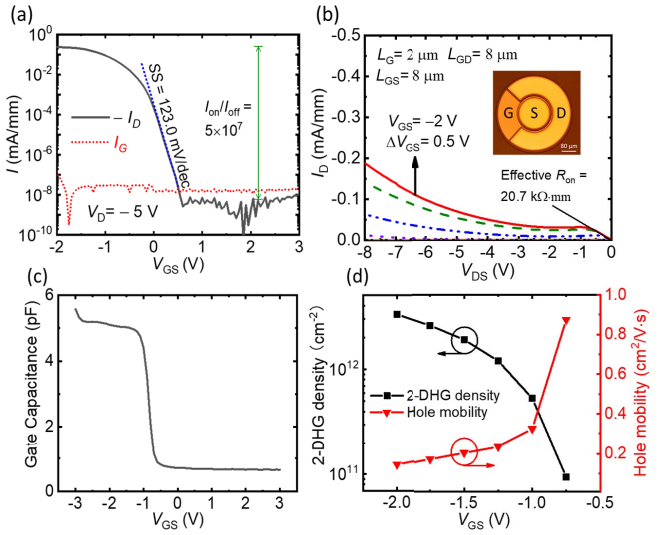

Fig. 3. (a) Transfer characteristics of the *p*-channel HFET in a semi-log scale demonstrating an off-current of $<10^{-8}$ mA/mm, ON/OFF ratio of 5×10^7, and *SS* of 123.0 mV/dec. (b) Output characteristics of the device demonstrating effective R_{ON} of 20.7 kΩ·mm. (c) Measured gate capacitance as a function of gate bias. (d) The relationship between the 2-DHG density, hole mobility and the applied gate bias.

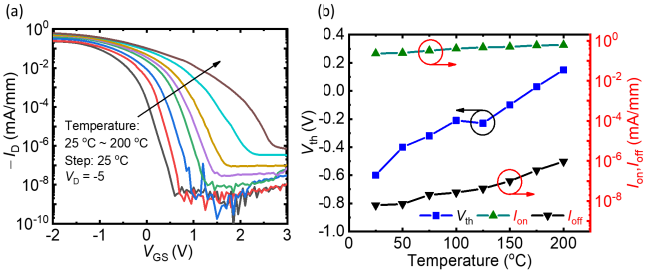

Fig. 4. (a) Temperature-dependent transfer curves of the *p*-channel GaN HFETs form 25 °C to 200 °C. (b) V_{th}, ON-current, and OFF-current of the devices as a function of temperature.

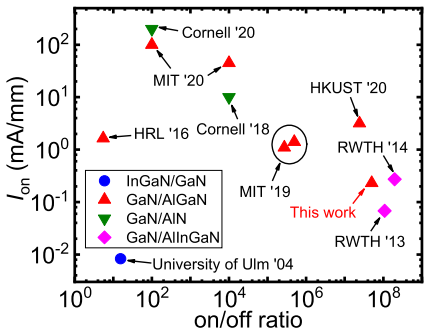

Fig. 5. Benchmark of the *p*-channel GaN HFETs extracted at $V_D = -5$ V. The shape of the data points represents device platforms. The institutes and publication years are also labeled for each report.

and 10 times smaller than previous results [12]. This is beneficial for the low power consumption required by the GaN CMOS implementation. The *SS* of the devices was 123.0 mV/dec, which is also the lowest *SS* ever reported for *p*-channel transistors on GaN/AlGaN platform, compared with the 400 mV/dec in [9] and 230 mV/dec in [12]. The improved performance on drain leakage and *SS* are attributed to the low-damage nature of the hydrogen plasma treatment process and the high-quality passivated *p*-GaN. The measured output curve is shown in Fig. 3(b) with effective ON-resistance (R_{ON}) at 20.7 kΩ·mm. The anomalous increase of drain current in saturation regime may be attributed to the 'kink effect', which is due to the impact-ionization-generated holes in the passivated *p*-GaN region [28].

The gate capacitance measurement was also performed, as shown in Fig. 3(c). The 2-DHG density and hole mobility as a function of gate bias were calculated using the method demonstrated in [29] and plotted in Fig. 3 (d). These values are lower than that measured by Hall before processing (11.9 $cm^2/V{\cdot}s$). This could be explained by two possible mechanisms: the vertical field could have increased the carrier scattering in the channel, and/or some over-diffused hydrogen atoms may adversely affect the hole mobility.

Figure 4(a) presents the temperature-dependent transfer curves of the device. The ON-current, off-state current and V_{th} increased with the temperature from 25 °C to 200 °C, as shown in Fig. 4(b). These changes may be due to the ionization of Mg in the channel at elevated temperatures [30]. The device maintained a decent ON/OFF ratio of 8×10^5 even up to 200 °C, which is also the highest reported temperature for GaN *p*-channel HFETs.

Figure 5 shows the benchmark plot of *p*-channel HFETs in terms of ON-current and ON/OFF ratio at V_{DS} of −5 V [6]–[12], [16], [31], [32]. Compared with previous reports, this work exhibits the lowest off-state leakage and *SS*, and the highest ON/OFF ratio among *p*-channel HFETs using the GaN/AlGaN platform. The ON-current can be improved by increasing the Al composition of the barrier [7], shrinking the channel length [31], [32] and inserting a UID-GaN layer between the *p*-GaN and the barrier [9]. These methods have been proven effective by previous studies and are compatible with the hydrogen plasma treatment process. The hydrogen plasma treatment is effective in suppressing leakages while preserving the excellent material quality of the *p*-channel.

IV. Conclusion

In summary, high-performance E-mode *p*-channel HFETs were realized on a commercially available *p*-GaN/AlGaN/GaN HEMT platform. The conventional gate recess via dry etching was replaced by a novel hydrogen plasma treatment, eliminating the dry etching-induced damage and trap states in the channel. A record low off-state leakage of 10^{-8} A/mm and a record low *SS* of 123.0 mV/dec were obtained. These results show that the hydrogen plasma treatment is effective in suppressing leakage and producing high-quality *p*-channel, a step closer to the high performance GaN complementary ICs.

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