Applied Physics Letters

RESEARCH ARTICLE | APRIL 22 2024

Device and material investigations of GaN enhancement-mode transistors for Venus and harsh environments

Special Collection: (Ultra)Wide-bandgap Semiconductors for Extreme Environment Electronics

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Appl. Phys. Lett. 124, 172104 (2024)
https://doi.org/10.1063/5.0186976

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Applied Physics Letters ARTICLE pubs.aip.org/aip/apl

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Cite as: Appl. Phys. Lett. **124**, 172104 (2024); doi: 10.1063/5.0186976
Submitted: 9 November 2023 · Accepted: 6 April 2024 ·
Published Online: 22 April 2024

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Note: This paper is part of the APL Special Collection on (Ultra)Wide-bandgap Semiconductors for Extreme Environment Electronics.
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ABSTRACT

This Letter reports the device and material investigations of enhancement-mode p-GaN-gate AlGaN/GaN high electron mobility transistors (HEMTs) for Venus exploration and other harsh environment applications. The GaN transistor in this work was subjected to prolonged exposure (11 days) in a simulated Venus environment (460 °C, 94 bar, complete chemical environment including $CO_2/N_2/SO_2$). The mechanisms affecting the transistor performance and structural integrity in harsh environment were analyzed using a variety of experimental, simulation, and modeling techniques, including *in situ* electrical measurement (e.g., burn-in) and advanced microscopy (e.g., structural deformation). Through transistor, Transmission Line Method (TLM), and Hall-effect measurements vs temperature, it is revealed that the mobility decrease is the primary cause of reduction of ON-state performance of this GaN transistor at high temperature. Material analysis of the device under test (DUT) confirmed the absence of foreign elements from the Venus atmosphere. No inter-diffusion of the elements (including the gate metal) was observed. The insights of this work are broadly applicable to the future design, fabrication, and deployment of robust III-N devices for harsh environment operation.

Owing to inherent limitations of Silicon technologies [e.g., bulk CMOS and silicon-on-insulator (SOI)], Gallium Nitride (GaN) electronics have been identified as a leading candidate, along with silicon carbide (SiC), for harsh environment applications in industry, planetary exploration, and hypersonic vehicles.[1–3] In addition to demonstrations of discrete III-N transistors across extreme temperatures (from 4 K to 1000 °C),[4–7] much attention has also been paid to GaN-based circuits, mostly for high temperature, based on D-mode n-FETs,[8,9] E/D-mode n-FETs,[10–13] and E-mode complementary (n + p) FETs[14–16] (D: depletion; E: enhancement; FET: field-effect transistor).

Long-term robustness and reliability studies are much needed to evaluate the performance of GaN electronics in practical harsh environments and to provide insights for their thermal hardening.[17,18] Many works have examined the degradation mechanisms of D-mode III-N HEMTs at high temperature (HT).[19–25] Preliminary robustness studies of E-mode p-GaN-gate HEMTs (typically < 300 °C, the SOI rating) have indicated promising potential of these transistors,[26–28] in addition to their demonstrated performance in power[29–32] and RF applications.[33,34] Considering that E-mode transistors are key in GaN-based integrated circuits (ICs)[35,36] and are more complex than D-mode HEMTs, more efforts are required to investigate the performance and degradation of these transistors in extreme environments beyond the SOI rating.

This Letter reports the investigations of E-mode p-GaN-gate AlGaN/GaN HEMTs for harsh environment operation from device and material perspectives. The proposed transistor [Fig. 1(a)] features a self-aligned refractory metal (tungsten, W)/p-GaN gate and is based on a p-GaN platform, which could support state-of-the-art GaN n-FET-based HT ICs,[37,38] an experimentally calibrated IC simulation framework,[39] and GaN complementary transistors.[40,41] Furthermore, the proposed transistor has been demonstrated to operate in a simulated Venus ambient (460 °C, 94 bar, complete chemical environment including $CO_2/N_2/SO_2$) for more than 10 days.[42] Building upon the initial promising demonstrations,[42,43] a comprehensive investigation of the proposed transistor would be highly valuable to understand the mechanisms affecting its performance and structural integrity in such operating conditions. To this end, the following aspects are investigated in this work: (1) the origins of the temperature-dependent electrical characteristics of the proposed transistor, specifically the ON-resistance R_{ON}; (2) packaging for *in situ* electrical testing; (3) microstructural characterization of the transistor (gate region) after the test;[44] and (4) chemical composition and structural integrity of the DUT after the test.

Three different epitaxial samples were used in this study. Sample 1 was optimized for E-mode transistor fabrication, and its epitaxial structure is presented in Fig. 1(a). In addition, the impact of the substrate at HT was studied in Samples 2 and 3. Sample 2 consists of

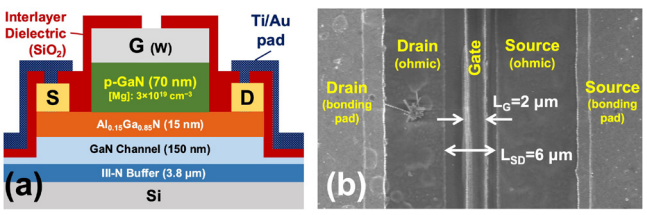

FIG. 1. (a) Schematic of the p-GaN-gate AlGaN/GaN HEMT studied in this work. (b) Scanning electron microscopy (SEM) image of the fabricated transistor.

$Al_xGa_{1-x}N$ (25 nm, $x = 0.25$)/GaN epitaxy on high resistivity (HR, rated > 5 kΩ·cm at room temperature) Si (111) substrate. Sample 3 consists of $Al_xGa_{1-x}N$ (18 nm, $x = 0.25$)/GaN epitaxy on semi-insulating (s.-i.) 4H-SiC substrate. Sample 1 was used for the fabrication of the proposed transistor [Fig. 1(b)], while Samples 2 and 3 were used for transport studies using Transmission Line Method (TLM) and van der Pauw structures, respectively. Details of the epitaxial structures and the process flow of the transistor are available in the supplementary material, Sec. I. The breakdown voltage of a similar transistor structure (on a similar epitaxial layer, without the inclusion of electric field management structures) is 50 V for $L_{GD} = 450$ nm.[41]

The comprehensive study of the proposed transistor (fabricated on Sample 1) begins with the analysis of the temperature dependency of electrical performance. Figure 2(a) presents the output characteristics of a representative transistor (bare die measured on a thermal chuck in a probe station) vs temperature. R_{ON}, a key metric for power switches and analog mixed-signal circuits, increases monotonically with temperature [Fig. 2(b)].

To understand the temperature dependency of R_{ON}, TLM structures were fabricated on Sample 2. Despite the slight difference in the alloy composition and thickness of the AlGaN barriers between Samples 1 and 2, the temperature dependency trends are expected to be similar. This is considering that polar optical phonon (POP) scattering is the dominant mechanism with temperature dependency [as will be shown in Fig. 2(h) inset], and POP scattering is a weak function of the Al composition.[45,46] TLMs were measured on a thermal chuck in a probe station (in Earth atmosphere) [Figs. 2(c) and 2(d)].

In addition, Hall-effect measurement (in vacuum) was conducted using van der Pauw structures fabricated simultaneously on Samples 2 and 3. Details of the Hall-effect measurement are reported in the supplementary material, Sec. II. Hall-effect measurement data based on Sample 2 was not used in this study because of the significant increase in the thermal generation of carriers in HR (room temperature-rated) Si substrate at HT. The free carriers in the substrate would flow to the Ohmic contacts located at the edges of the sample (in a van der Pauw structure geometry), therefore contributing to the measured Hall current and resulting in a "measurement artifact."

On the other hand, this measurement artifact is not observed in van der Pauw structures fabricated on Sample 3 (s.-i. SiC substrate). As shown in Fig. 2(e), at HT (at least up to 400 °C), the sheet charge density n_{sh} remains largely constant (variation of $< 5 \times 10^{11}$ cm^{-2}) and is consistent with other reports.[47] The comparison between Samples 2 and 3 (similar AlGaN/GaN epitaxy but different substrates) suggests that the substrate is the likely cause of the discrepancy in the Hall-effect measurement. Future improvements to the van der Pauw structure, e.g., by moving the Ohmic contacts slightly inwards of the sample would likely circumvent this issue.[47] The mobility μ from Hall-effect measurements of this work shows a significant decrease. Excellent agreement was obtained between the sheet resistance R_{sh} values extracted from TLM and Hall-effect measurements [Fig. 2(f)].

The (ON-)resistance values extracted by the three above-mentioned methods were compared in Fig. 2(g). Given that the transistor is long-channel ($L_{SD} = 6\,\mu$m), the contact resistance constitutes a small percentage of the total resistance (<10%) and could be neglected for the purpose of this analysis. Furthermore, this work focuses on the relative trends of R_{sh}. Both the gated region and the non-gated (access) region experience mobility decrease at HT primarily by POP scattering. These

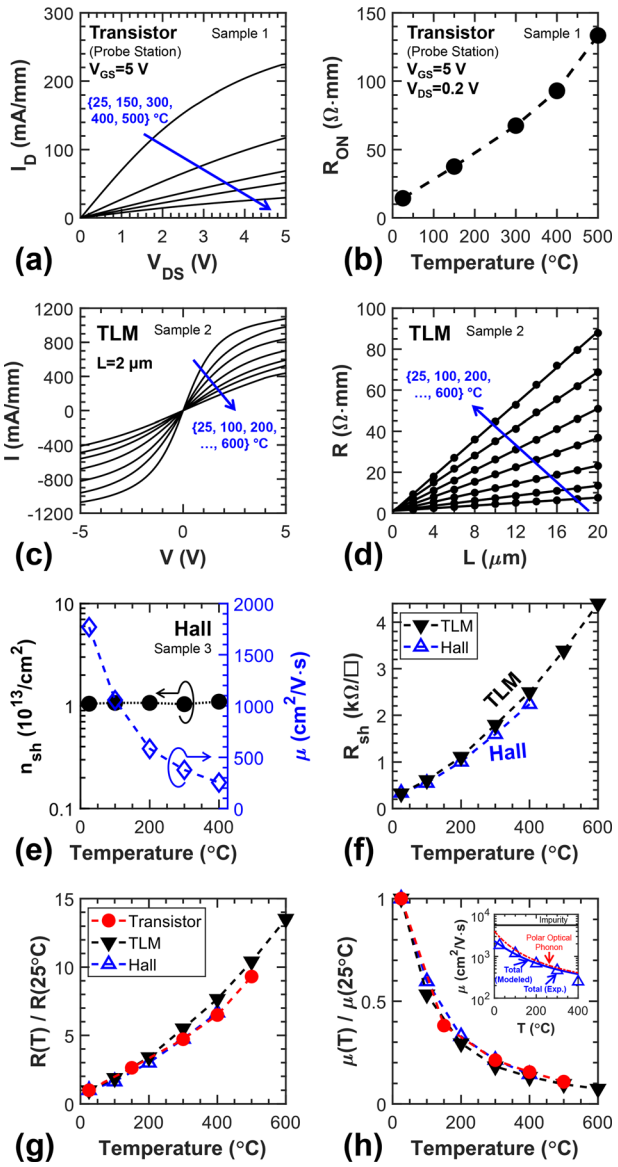

FIG. 2. Investigation of transistor characteristics vs temperature. (a) Output characteristics of the transistor (Sample 1) measured in the probe station. (b) Transistor (Sample 1) R_{ON} extracted at $(V_{GS}, V_{DS}) = (5, 0.2)$ V. (c) I–V characteristics of a TLM structure (Sample 2) measured in the probe station. (d) TLM (Sample 2) R vs L (solid symbols). The line of best fit (drawn as a guide to the eye) is used to extract R_{sh}. (e) Hall-effect measurement of van der Pauw structures (Sample 3). (f) Comparison of R_{sh} extracted from TLM and Hall-effect measurements. (g) Comparison of resistance $R(T)$ (normalized by the value at 25 °C) extracted by various measurements. (h) Comparison of $\mu(T)$ (normalized by the value at 25 °C) extracted by various measurements. A basic modeling of the scattering mechanisms for mobility is shown in the inset.

considerations are reinforced by the close fit among the HT trends of R_{ON} of the transistor, and the R_{sh} extracted from TLM and Hall-effect measurements (normalized by their respective values at 25 °C) (e.g., at 500 °C, 12% discrepancy between the transistor and TLM values).

A similar comparison was conducted on electron mobility μ. Here, the transistor and TLM values are extracted assuming $\mu \propto 1/R$ [from Figs. 2(b) and 2(f)] and constant n_{sh} vs T. The Hall values are taken from the raw data [Fig. 2(e)]. At HT, a close fit is obtained in the values of $\mu(T)/\mu(25°C)$: between the transistor and TLM, 10.6% discrepancy at 500 °C; between the transistor and Hall, 6.9% discrepancy at 400 °C. The close fit among these datasets suggests that mobility decrease is the primary cause of the increase in R_{ON} and, consequently, decrease in $I_{D,max}$ in the transistor at HT. It should be noted that there is a slight change in threshold voltage V_{TH} of the transistor (by ~ 0.32 V);[42] therefore, R_{ON} was used and extracted at high gate overdrive ($V_{GS} - V_{TH} > 3.5$ V). Furthermore, other non-idealities in the gated region of the transistor, e.g., surface states, may lead to changes in the current conducting capability at HT.

It is insightful to verify the key scattering mechanisms affecting electron mobility in the sample. The Hall measurement data were used in a basic modeling of the scattering mechanisms, which include impurity scattering (assumed to be independent of temperature) and POP scattering. An excellent fit was obtained from 25 to 400 °C, as shown in Fig. 2(h), inset. The result verifies that POP scattering is the dominant mechanism for temperature dependency of mobility at HT and is in agreement with earlier studies.[48] The modeling is presented in detail in the supplementary material, Sec. III. Using the mobility model, the mobility trend $\mu(T)/\mu(25°C)$ was extrapolated to 500 °C (highest temperature measured of the transistor) (not shown). A good fit was again obtained among the datasets, therefore suggesting that increased POP scattering is the major cause for R_{ON} increase in the reported transistor at HT.

The DUT was exposed to a simulated Venus environment in the NASA Glenn Extreme Environments Rig (GEER).[49] *In situ* electrical measurement of the DUT was enabled by a custom-built measurement setup.[43] The bare die was packaged using HT rated components (e.g., alumina printed circuit board (PCB), 10 mil gold wires shielded by ceramic beads), as shown in Figs. 3(a)–3(c). As illustrated in Fig. 3(d), at the beginning of the test, the $I_{D,max}$ of the packaged DUT does not vary smoothly with increasing temperature. Three representative time instances (i)–(iii) are identified in Fig. 3(d), with the corresponding I–V curves presented in Fig. 3(e). It should be noted that a fresh device was used as the DUT. Other devices fabricated in the same batch showed similar performance in the intrinsic transistor (as measured in a probe station), with good uniformity in the devices located across the sample.[38,42] Therefore, the cause of the above-mentioned behavior in the DUT at the beginning of the test [Fig. 3(d)] was attributed to "burn-in."

Initially, when the chamber was at room temperature, the measured $I_{D,max}$ hovered at ~10 mA/mm, as is represented by time instance (i) [Fig. 3(e)(i)]. The triode regime (low V_{DS}) exhibited a Schottky turn-on behavior. As the temperature was increased linearly over time (together with pressure which also increased linearly over time), $I_{D,max}$ decreased, as represented by time instance (ii) [Fig. 3(e)(ii)]. The wire bonding had not been exposed to sufficiently high temperature and/or for a sufficiently long duration for the wire bonds to form the best contact. The decrease in measured $I_{D,max}$ is attributed to the decrease in $I_{D,max}$ of the intrinsic transistor, due to a decrease in mobility. However, the non-ideal wire bond still remained, leading to the extremely low current. At time instance (iii), or day −1.5, the current suddenly increased, and good transistor I–V behavior was observed

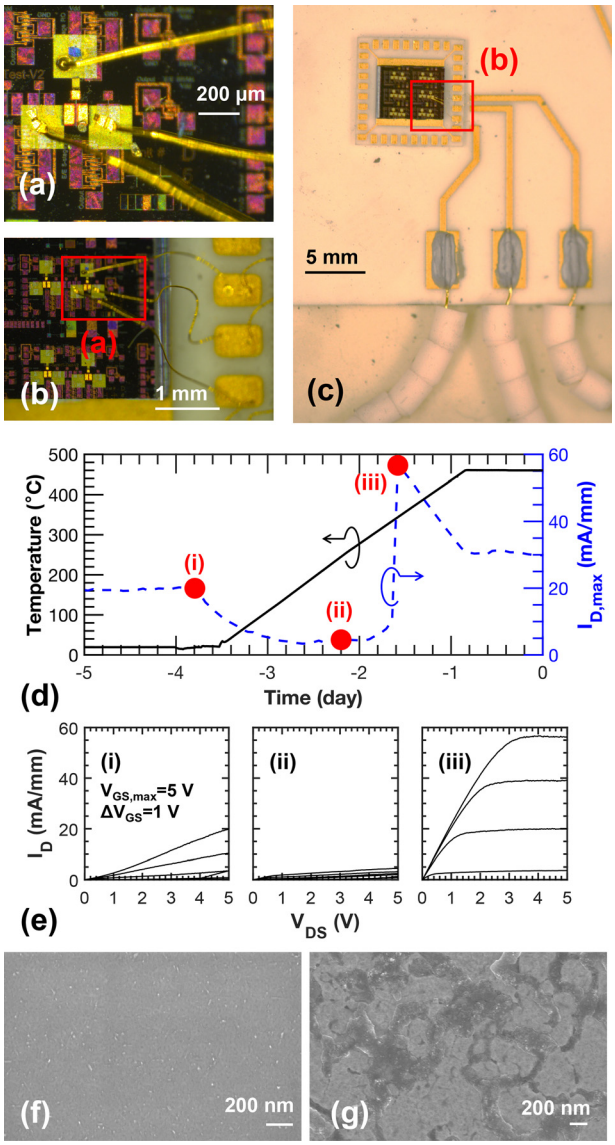

FIG. 3. Wire bonding of the DUT and the burn-in effect. (a) Optical image of the DUT. Gold wires are bonded to each of the three electrodes. (b) Attachment of the sample containing the DUT on the alumina PCB. The other end of the bond wire is connected to the electrodes on the PCB. (c) Overview of the alumina PCB. The wires of the PCB are connected to the rest of the measurement setup. (d) Temperature and $I_{D,max}$ of the DUT (from the GEER measurement setup) over time. Day 0 refers to the stabilization of DUT performance and start of robustness study, in accordance with the authors' earlier report.[42] (e) Output characteristics of the DUT at various time instances, as indicated by the red dots in (d). (f) and (g) SEM images of the gold bonding pad before and after the test, respectively.

[Fig. 3(e)(iii)]. The improvement in performance of the DUT is attributed to the completion of the burn-in, where excellent electrical contact has been formed between the gold pad (of the DUT) and the bonding wire. After the test, the Ti/Au bonding pad was alloyed, and some metal segregation was observed [Figs. 3(f)–3(g)]. For the future work, annealing pretreatment could be applied to the packaging to ensure that a low-resistance electrical connection is achieved in the wire bonding.

At the end of the simulated Venus test (cooldown from 460 °C), $I_{D,max}$ of the DUT rose by 3.9 times at 50 °C (compared to 460 °C), whereas the probe station measurements (in Earth atmosphere) would predict an increase by five times. The discrepancy, as illustrated in Fig. 4, implies some level of degradation in the DUT. Therefore, besides the alloying of the bond pad, other potential sources of degradation will be investigated next. It should be noted that the probe station measurements were done in a much shorter duration (2 h) because the small thermal chuck heated up and stabilized quickly; for the simulated Venus test, the GEER is a large vessel, and simulated Venus exposure took place for 11 days. Therefore, the gate degradation is not expected to be a significant issue for the DUT during the probe station measurements.

A major issue is the partial structural degradation of the gate region, which was reported in the authors' earlier study.[42] Figure 5(a) depicts the gate region of a fresh device. The gate metal (W) exhibits good adhesion to the surface of p-GaN. On the other hand, after exposure to the simulated Venus environment, the gate metal in the DUT is partially detached, leaving behind only the middle portion intact to the p-GaN [Fig. 5(b)]. Furthermore, cracks were found in the SiO_2 surrounding the gate metal [Figs. 5(c) and 5(d)]. The intrinsic stress in the deposited material is expected to contribute to the degradation. To circumvent this issue, the SiO_2 deposition was optimized for zero stress, and the W deposition recipe was optimized for a combination of low resistivity and reasonable (tensile) stress.

The observed crack in the gate region is largely attributed to the difference in the coefficients of thermal expansion (CTEs) between SiO_2 and W. For reference, the reported CTE values for SiO_2 and W are 0.6×10^{-6}/°C and 4.45×10^{-6}/°C, respectively (over the range of 25–400 °C).[50,51] Finite-element method (FEM)-based simulation of the gate structure was conducted using COMSOL Multiphysics. As illustrated in Fig. 5(e), the gate structure is deformed after being exposed to the simulated Venus atmosphere (from the Earth atmosphere). Similarities in the shape of the deformation are observed between the simulation [Fig. 5(e)] and the device after test [Figs. 5(b)–5(d)]. It is

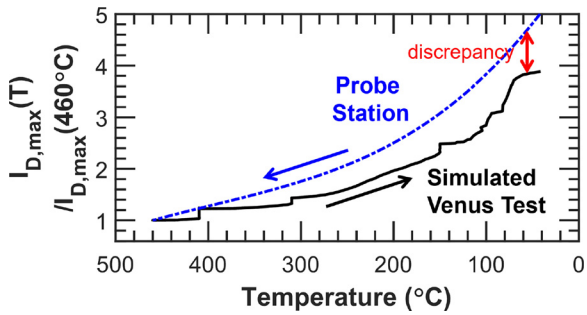

FIG. 4. Rise in $I_{D,max}$ (normalized) of DUT after simulated Venus conditions (DUT was cooled down from 460 °C). The value of $I_{D,max}$ (interpolated and normalized) as measured in the probe station (DUT was heated up from 25 °C) is overlaid. The discrepancy in $I_{D,max}$ values reveals that the DUT could not achieve full recovery to its $I_{D,max}$ at room temperature. (Note: The spikes in $I_{D,max}$ vs temperature in the simulated Venus test correspond to the purges during the cooldown of the chamber. After 150 °C, the chamber was purged of the Venus gas mixture and subjected to natural cooling.)

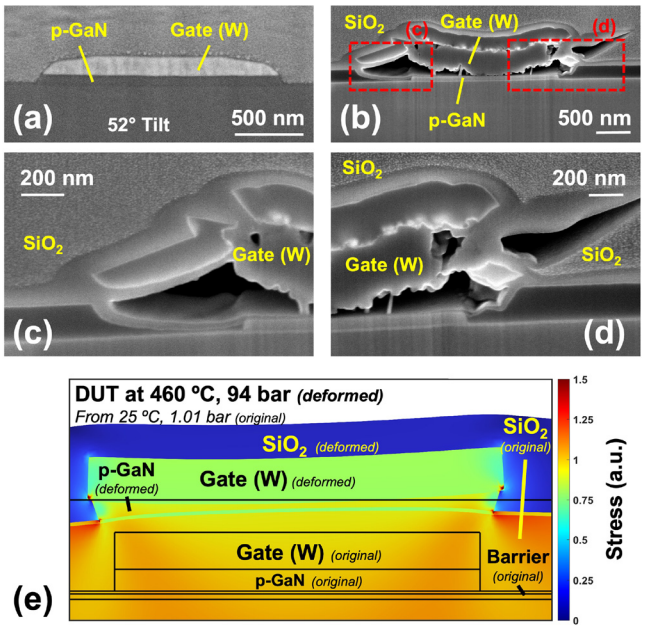

FIG. 5. Investigation of the structural degradation in the gate region. (a) Cross-section (focused ion beam cut) of the gate region of a similar device immediately after fabrication, without the simulated Venus exposure. (b) SEM of the gate region of the DUT after the simulated Venus exposure. (c) and (d) Zoom-in views of the gate region of the DUT. (e) Simulation of the structural change in the gate region at simulated Venus temperature and pressure ("deformed"), as compared to (Earth) room temperature and pressure ("original"). The black lines indicate the original structure. The position of the corresponding colored regions indicates the displacement in the deformed structure, while the color map indicates the magnitude of stress.

likely that the exposure to harsh environment (Venus) induced nonreversible degradation to the structure (e.g., inelastic degradation of the SiO_2 layer). Therefore, after the device was cooled down to room temperature, the structure could not be recovered to the initial state in Earth atmosphere [Fig. 5(a)]. Instead, bending and cracks were found in the device [Figs. 5(b)–5(d)]. The results indicate the need for minimal-stress thin films in the device (especially for structures with surface topology, like the SiO_2 layer which surrounds the p-GaN island), choice of films with less CTE mismatch, and high quality films (e.g., dense SiO_2 films) with good adhesion to surfaces, to avoid cracks as much as possible. Details of the simulation of the gate structure are presented in the supplementary material, Sec. IV.

The DUT was investigated for any chemical change occurred in the material, either the addition of foreign elements (e.g., from the ambient[43]) or the spatial diffusion of the elements due to the prolonged exposure to high temperature and pressure. Energy-dispersive x-ray spectroscopy (EDS) of the DUT indicates that the common elements are found, as expected [Fig. 6(a)]. A detailed EDS of each element and the EDS integrated spectrum are found in the supplementary material, Sec. V.

The presence of highly reactive gases (e.g., SO_2) poses significant challenges to the device. In an earlier report regarding the exposure of GaN p-n diodes in a simulated Venus environment (same conditions as in this work), significant sulfurization of Pd/Ni/Au (anode metal)

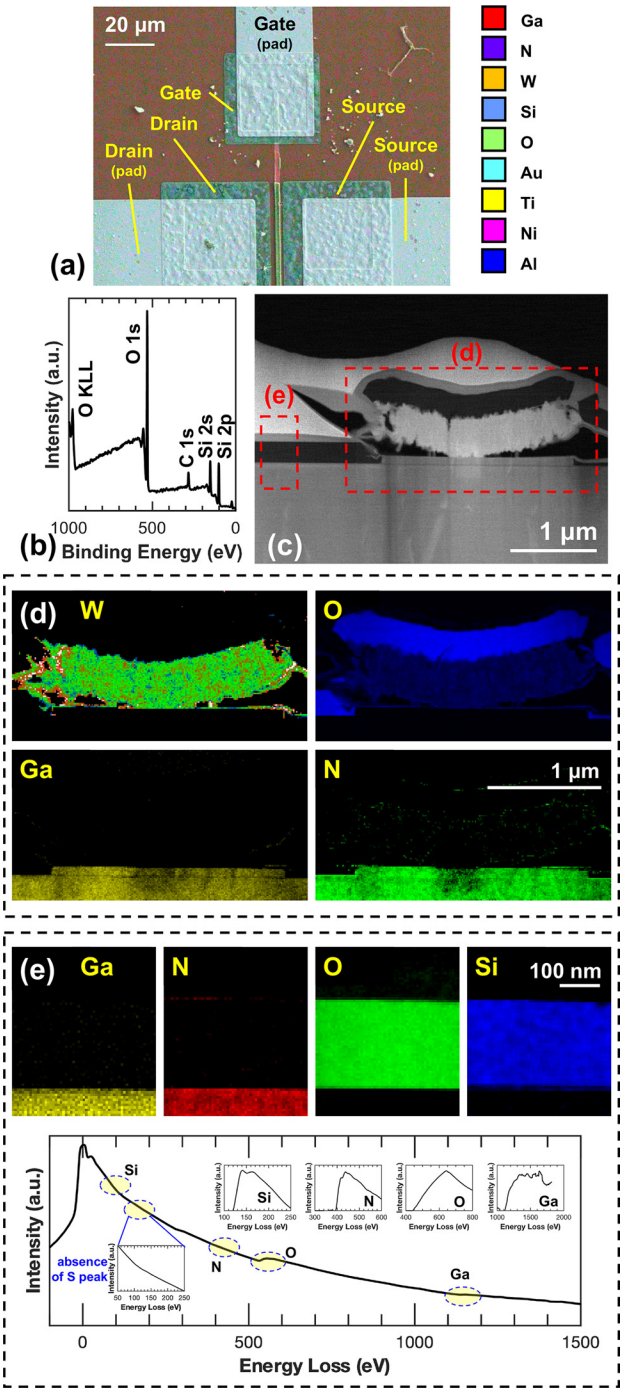

FIG. 6. Chemical composition of the DUT. (a) EDS image (false color) of DUT with the colored dots indicating the dominant element (EDS images of all elements and the EDS integrated spectrum are available in the supplementary material, Sec. V). (b) XPS of the surface of the DUT. (c) Cross-section of the DUT for EELS analysis. (d) EELS mapping of the gate region. (e) EELS mapping of the access region. Insets of the spectrum (integrated intensity) show the signals of the individual elements (Si, N, O, and Ga) and the absence of an S peak. Note that the intensity values of the main EELS spectrum (but not the insets) are plotted in logarithmic scale.

was observed. Degradation of electrical performance was, thus, observed.[52] In this work, the intrinsic DUT (source, drain, and gate metals and the transistor channel) was protected by a SiO_2 layer. No trace of S was detected by EDS at the currently used EDS parameters. Note that the detection range of EDS is $>1.5\,\mu$m (well into the GaN buffer region) for an accelerating voltage of 15 kV.

In order to further trace the presence of S in the device after test, x-ray photoelectron spectroscopy (XPS) and electron energy loss spectroscopy (EELS) were employed. XPS could provide intricate information about the surface elemental composition because XPS has a significantly higher detection limit than EDS.[53–55] As shown in Fig. 6(b), the obtained XPS results clearly show peaks of Si and O corresponding to the protective layer of SiO_2 covering the intrinsic DUT and indicate the absence of S element. Similarly, EELS is another promising elemental analysis technique owing to its high spatial resolution and sensitivity,[56,57] and has been routinely used to study structural degradation in GaN and other devices.[23,58] Therefore, EELS analysis was conducted on the cross-sectional region [Fig. 6(c)], which includes the gate region and access regions [Figs. 6(d) and 6(e), respectively]. No inter-diffusion of the layers was observed. This absence of inter-diffusion in the gate metal is attributed to the use of refractory metal, whereas significant inter-diffusion occurred in non-refractory metal electrodes of devices after harsh environment exposure.[23,52] The combined elemental study (XPS and EELS) confirms that no trace of S was found in the DUT. The results indicate the importance of a protective layer for effective shielding of the device from foreign material/environment (e.g., SO_2, a highly reactive gas).

In conclusion, the enhancement-mode p-GaN-gate AlGaN/GaN HEMT was investigated for harsh environment operation from the device and material perspectives. A variety of mechanisms affecting the performance and structural integrity of the proposed transistor were analyzed. Through a comparison of transistor, TLM, and Hall-effect measurement results, it is revealed that reduced mobility (from increased POP scattering) is the primary cause of reduction of ON-state performance of the proposed transistor at HT. Several sources of non-idealities were analyzed, e.g., burn-in of wire bonding and microstructural degradation in the gate region (verified by simulation). Extensive material characterization (EDS, XPS, and EELS) confirmed the effectiveness of SiO_2 in protecting the intrinsic transistor and the absence of inter-diffusion among the elements. The insights of this work are broadly applicable to the future design, fabrication, and deployment of III-N devices for harsh environment operation.

See the supplementary material for detailed information on (1) the epitaxial structure and process flow of the DUT, (2) Hall-effect measurements, (3) analysis of mobility decrease at HT through modeling of scattering mechanisms, (4) simulation of gate deformation at HT, and (5) the microscopy and material analysis of the DUT.

This work was sponsored in part by the National Aeronautics and Space Administration (NASA) Hot Operating Temperature Technology (HOTTech) Program under Grant No. 80NSSC17K0768 (monitored by Dr. Gary W. Hunter); the Air Force Office of Scientific Research (AFOSR) under Grant No. FA9550-22-1-0367 (monitored by Dr. Kenneth C. Goretta); Lockheed Martin Corporation under Grant No. 025570-00036 (monitored by Dr. John J. Callahan); Samsung Electronics Co., Ltd. under Grant No. 033517-00001 (monitored by Dr. Jongseob Kim); ULTRA, an Energy Frontier Research Center through the U.S. Department of Energy (DOE) Office of Science, Basic Energy Sciences (BES), under Grant No. DE-SC0021230; CHIMES, one of the Seven Centers in JUMP 2.0, a Semiconductor Research Corporation (SRC) Program by DARPA; and Bangladesh University of Engineering and Technology (BUET). The authors gratefully acknowledge Dr. Kai Cheng of Enkris Semiconductor, Inc. for the provision of the epitaxial wafers; Dr. Philip G. Neudeck, Dr. Liangyu Chen (concurrently with Ohio Aerospace Institute), Mr. Nathan W. Funk, Mr. Joseph E. Rymut, Mr. Mark D. Sprouse, Mr. Daniel G. Gerges, Mr. John D. Wrbanek, Mr. Craig Motil, and Mr. Ian Henry of NASA Glenn Research Center for assistance in the harsh environment testing; and Makel Engineering, Inc. for the packaging. Device fabrication was conducted at MIT.nano, Massachusetts Institute of Technology.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Qingyun Xie and John Niroula contributed equally to this work.

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DATA AVAILABILITY

The data that support the findings of this study are available within the article and its supplementary material.

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